60-nm Gate Length SOI CMOS Technology Optimized for “System-on-a-SOI-Chip” Solution


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Abstract

In this paper, we describe 60-nm gate length SOI CMOS technology for “system-on-a-SOI-chip” solution. This concept features that: 1) high speed logic circuits are designed with PDSOI in order to enhance operation speed, 2) the remaining circuits which require stable body potential are designed with body-slightly-tied SOI (BSTSOI™), in which body potential is fixed with no area penalty. With newly developed self-aligned dual trench isolation (SDTI), both PDSOI and BSTSOI can be fabricated on the same die. We compare PDSOI and BSTSOI with bulk CMOS devices in terms of transistor characteristics and circuit performance including SRAM static noise margin as well as soft error immunity. In addition, we demonstrate stacked metal-insulator-metal (MIM) capacitor DRAM cell fabricated on BSTSOI.

Introduction

System-on-a-chip technology is the key solution for high-speed and low power operation requirement, and partially depleted (PD) SOI is a very promising technology for device performance improvement due to smaller junction capacitance and floating body effect. Especially floating body enables high-speed operation with enhanced drive current and reduced body-bias effect. However, floating body effect also induces hump in output characteristics and history effect in ac operation, which cannot be tolerated for use in high-voltage I/O, analog circuits, and several critical circuits. To solve this issues, T-gate structure has been proposed to achieve body-contacted SOI. However the additional gate capacitance imposed by T-gate is undesirable. Moreover, it is not practical for SRAM or DRAM cell because of area penalty. SOI/bulk hybrid substrate, which has both SOI region and bulk region, is a good candidate to solve the above issue [1-3], but it increases both process complexity and cost.

In this paper, we describe 60-nm gate length SOI CMOS technology optimized for system-on-a-chip solution. In order to solve the body-contact issue, we utilized body-slightly-tied (BST) SOI [4], which features partial trench isolation [5-6]. BSTSOI shows negligible floating body effect, indicating that existing circuit and layout design of bulk CMOS are reusable while enjoying lower junction capacitance. Moreover, we have developed self-aligned dual trench isolation (SDTI), which allows the fabrication of both PDSOI and BSTSOI on the same die. As the result of this, high-speed logic circuits can be designed with PDSOI in order to enhance operation speed, while high-voltage I/O and
analog circuits can be designed with BSTSOI in order to obtain stable body potential. We compare PDSOI and BSTSOI with bulk CMOS in terms of transistor characteristics and circuit performance including SRAM static noise margin as well as soft error immunity. We have also fabricated stacked metal-insulator-metal (MIM) capacitor DRAM cell [7] on BSTSOI.

Fig.1: System-on-a-SOI-chip concept. High-speed logic circuits are designed with PDSOI and high-voltage I/O, analog, and memory cells are designed with BSTSOI.

Device structures and isolation technology

Fig.2 shows a schematic diagram of BSTSOI and PDSOI device structures with self-aligned dual trench isolation (SDTI). PDSOI device is surrounded by full trench isolation which reaches buried oxide (BOX) layer, and body of PDSOI is electrically isolated. On the other hand, BSTSOI device is surrounded by partial trench isolation, in which SOI layer remains between BOX layer and trench isolation. Therefore body potential of BSTSOI is fixed with body contact via resistance path below the trench isolation. We can reuse most of existing circuit and layout design of bulk CMOS in BSTSOI.

Fig.2: BSTSOI and PDSOI device structures. PDSOI device is isolated by full trench isolation, and BSTSOI device is surrounded by partial trench isolation.
Fig. 3 schematically shows process sequence of SDTI. Here initial SOI thickness was 150 nm. First, partial trench (etching depth of 100 nm) was formed followed by thermal liner oxidation. Next, sidewall spacer was formed. Then, p-well and n-well implantations for BSTSOI region were performed. These implantations lower well resistances under partial trench, and enable isolation space (n⁺ to n⁺ or p⁺ to p⁺) shrinking in BSTSOI region. Then full trench, self-aligned with partial trench isolation by sidewall spacer, was formed. There is no waste space region between partial and full trench isolation boundary as shown in Fig. 4.

Transistor fabrication process after SDTI was based on 90-nm node bulk CMOS technology with dual gate oxide process [8-10]. The equivalent oxide thickness of gate dielectric of core transistor was 1.6 and that of 1.8V I/O transistor was 3.5nm. The gate length of core transistor was 60 nm. The poly-SiGe gate and pre-doping technology were used to reduce gate-poly depletion. Spike RTA was used to improve both short channel effect and drive current. For comparison, we fabricated bulk, PDSOI, and BSTSOI CMOS with the same channel, S/D extension, and halo ion-implantation conditions. Fig.
Fig. 5 shows cross-sectional TEM of PDSOI MOSFET with SDTI. Final SOI film thicknesses under gate electrode and source/drain region were 130 nm and 115nm, respectively.

![Fig.5: TEM view of 60-nm gate length MOSFET. Gate electrode has Si/SiGe stacked poly structure.](image)

**Transistor characteristics**

**A) BSTSOI**

Fig. 6 shows n\(^+\)-n\(^+\) or p\(^+\)-p\(^+\) punch-through voltage of bulk and BSTSOI as a function of isolation space. Here, shallow trench isolation (STI) depth used in bulk is 300nm, while partial trench isolation depth used in BSTSOI is only 100nm. Higher well implantation dose improves isolation but at the same time increases STI-edge junction capacitance. In order to maintain punch-through voltage over 3V at minimum spacing of 0.14µm, we selected 7×10\(^{12}\) cm\(^{-2}\) boron implantation for n\(^+\) to n\(^+\) isolation, and 3×10\(^{12}\) cm\(^{-2}\) arsenic implantation for p\(^+\) to p\(^+\) isolation. With this condition, sheet resistance of 11.0×10\(^3\) ohm/sq for p-well and that of 9.5×10\(^3\) ohm/sq for n-well were obtained. These values are about 10 times higher than those of bulk.

![Fig.6: Punch-through voltage as a function of isolation space. BSTSOI has three different well implantation samples.](image)

Subthreshold characteristics of BSTSOI are compared with those of bulk in Fig.7. There is no difference between BSTSOI and bulk for both linear (V\(_{dd}\)=0.05V) and saturation (V\(_{dd}\)=1.0V) conditions. BSTSOI has no kink in I\(_d\)-V\(_d\) curves as shown in Fig.8. Drive current of bulk is 723µA/µm for n-channel MOSFET and 290µA/µm for p-channel MOSFET, while that of BSTSOI is 702µA/µm for n-channel MOSFET and 282µA/µm for p-channel MOSFET, at off leakage current of 30nA/µm and supply voltage of 1.0V. BSTSOI suffers from self-heating effect (SHE) as well as PDSOI. We estimated SHE of the BSTSOI using AC drain conductance method [11]. Temperature increase of n-channel MOSFET by SHE is 19.5°C and that of p-channel MOSFET is 9.5°C in BSTSOI, with gate length of 60 nm, gate width of 1.0 µm, and supply voltage is 1.0V. Corresponding
drain current degradations are estimated to be 2.3% for n-channel MOSFET and 1.1% for p-channel MOSFET. These values are smaller than PDSOI case, because body contact works as a heat spreader.

![Subthreshold characteristic diagram](image1)

Fig.7: Subthreshold characteristics of Bulk and BSTSOI devices with \( L_g = 60\text{nm} \). BSTSOI shows almost the same curves with those of bulk.

![Output characteristic diagram](image2)

Fig.8: Output characteristics of Bulk and BSTSOI devices with \( L_g = 60\text{nm} \). BSTSOI shows no kink in curves.

**B) PDSOI**

Subthreshold characteristics of PDSOI are compared with those of bulk in Fig.9. There is no difference between PDSOI and bulk with \( V_{dd} = 0.05\text{V} \). However, PDSOI shows larger DIBL and higher off leakage current with \( V_{dd} = 1.0\text{V} \). PDSOI has kink in output characteristics as shown in Fig.10. Drive current of PDSOI is \( 800\mu\text{A}/\mu\text{m} \) for n-channel MOSFET with off leak of \( 160\text{nA}/\mu\text{m} \) and \( 309\mu\text{A}/\mu\text{m} \) for p-channel MOSFET with off leak of \( 130\text{nA}/\mu\text{m} \). Drain current degradation of PDSOI by self-heating effect were estimated to be 2.7% for n-channel MOSFET and 1.3% for p-channel MOSFET with gate length of 60 nm, gate width of 1.0 \( \mu\text{m} \) at supply voltage of 1.0V.
Fig. 9: Subthreshold characteristics of Bulk and PDSOI with $L_g=60$nm. PDSOI shows larger DIBL with drain voltage of 1.0V.

Fig. 10: Output characteristics of Bulk and BSTSOI with $L_g=60$nm. PDSOI shows kink in curves.

Floating body effect causes larger DIBL (higher off current) and kink characteristics in PDSOI. Under dc bias condition, floating body reaches equilibrium potential when body-source forward current balances drain-body hole current generated by impact ionization and GIDL [12]. So, we can estimate floating body potential by monitoring body current at various forward body bias using body contacted device [13]. Fig. 11 shows estimated floating body potential of n-channel PDSOI as a function of drain voltage. When drain voltage is 1.0V, estimated body potential is 0.36V at gate voltage of 0V, and 0.51V at gate voltage of 1.0V. Hole current generated by impact ionization and GIDL strongly depends on drain voltage, therefore body potential drastically reduces with smaller drain voltage. Fig. 12 shows dependence of body potential on temperature. Body potential decreases with temperature increasing. This is because forward current from body to source increases proportionally with $\exp[-E_g/kT]$ and equilibrium potential decreases. These results are consistent with off current behavior with drain current or temperature as shown in Figs. 14 and 16.
Circuit performance

A) Propagation delays

Figs. 13 and 14 show propagation delays of inverter gate and off current (I_{off-sum}) as a function of supply voltage. I_{off-sum}, which means average off current measured in dc conditions, is defined as follows; I_{off-sum}=(W_n \times I_{offn} + W_p \times I_{offp})/(W_n + W_p); here W_n and W_p are gate width of n-channel and p-channel MOSFET used in inverter gate. When supply voltage is 1.0V, speed enhancement of PDSOI over bulk CMOS is 23%. However off current of PDSOI is 4.5 times higher than that of bulk device. Off current difference between bulk and PDSOI drastically reduced with lower supply voltage (supply voltage means drain voltage in this case). On the other hand, BSTSOI has almost the same off current with bulk device but its speed enhancement over bulk is 7.2%.

Figs. 15 and 16 show temperature dependence of propagation delay and off current for PDSOI and bulk devices. Off current difference of PDSOI and bulk devices decreases with temperature increase. In PDSOI, body potential becomes smaller with temperature increase as shown in Fig. 12, and reduces off current increase rate with temperature increase.

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Fig. 11: Body potential as a function of drain voltage for n-channel PDSOI.

Fig. 12: Body potential as a function of temperature for n-channel PDSOI.

Fig. 13: Propagation delays of inverter gate with F/O=1. L_g=60nm.

Fig. 14: I_{off-sum} versus supply voltage. I_{off-sum} is the average off current of inverter gate measured at dc condition.
Fig. 15: Propagation delays of inverter gate as a function of temperature.

Fig. 16: $I_{\text{off}}$-sum of inverter gate versus temperature. PDSOI shows 4.5 times higher $I_{\text{off}}$ at 25°C and 1.6 times higher $I_{\text{off}}$ at 110°C than bulk counterpart.

**B) SRAM characteristics**

We evaluated characteristics of SRAM cell with 130nm node design rule. SRAM cell is 2.39 $\mu$m$^2$, and supply voltage is 1.2 V. Fig. 17 shows butterfly curves of SRAM cells with PDSOI, BSTSOI and bulk devices. Static noise margin (SNM) of PDSOI is smaller than those of BSTSOI and bulk. This result can be explained as follows; PDSOI lower the threshold voltage of both driver gate and transfer gate. Moreover body bias effect of transfer gate in PDSOI is much smaller compared with BSTSOI or bulk, resulting in smaller drive current ratio of driver gate and transfer gate.

Soft error rate (SER) with alpha particle are compared among these devices as shown in Fig 18. Here, we used $p^+$ epitaxial layer on $p^+$ substrate as bulk devices. With SOI thickness of 150nm and supply voltage of 1.2V, SER of PDSOI shows 10 times smaller than that of bulk, and BSTSOI shows 30 times smaller SER than that of bulk. SOI devices exhibit higher soft error immunity than bulk, because the charge generation area is significantly reduced with thin SOI film. In addition, it has been reported that floating body nature of PDSOI itself reduces soft error immunity [12]. BSTSOI shows even higher soft error immunity than PDSOI, because body potential rise due to generated holes is well suppressed [14]. From the view point of SNM and SER, BSTSOI is the most preferable SOI technology for SRAM cell.

Fig. 17: Butterfly curves of SRAM cells with PDSOI, BSTSOI, and bulk devices.

Fig. 18: Soft error rate (SER) of SRAM cell as a function of supply voltage.
C) Embedded DRAM

Fig. 19 shows cross-sectional TEM photograph of DRAM cell on BSTSOI. This DRAM cell, which consists of salicided transistor and MIM capacitor, achieves extremely high-speed random access cycle of 570 MHz [7]. The body potential of DRAM cell is pinned with body contact so that bulk-based cell layout can be reused. Furthermore, there is no waste area between BSTSOI and PDSOI boundary so that part of peripheral circuits can be selectively designed with speed-enhancing PDSOI without area penalty.

![Fig. 19: Cross-sectional TEM photograph of embedded DRAM cell on BSTSOI. DRAM cell featured Co-salicided transistor and MIM capacitor. Cu interconnect was integrated with low-k “L-Ox™”.](image)

Conclusions

In this paper, we describe 60-nm gate length SOI CMOS technology optimized for system-on-a-chip solution. Self-aligned dual trench isolation technique enables integration of PDSOI and BSTSOI on the same die. PDSOI shows speed enhancement of 23% over bulk CMOS, while BSTSOI shows better static noise margin and higher soft error immunity of SRAM cell than PDSOI. We also demonstrated stacked MIM capacitor DRAM cell on BSTSOI.

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