A TH-UWB Transmitter and its Pulse Generation Circuit for Intra/Interchip Wireless Interconnection

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1. Introduction

Steady downsizing of semiconductor device dimensions has been the main stimulus to achieve higher speed and performance of integrated circuits over the past decades. Unfortunately scaling has a reverse effect on interconnect delay associated with the parasitic R, L, and C of conventional wiring. The introduction of low resistivity copper and low-permittivity (k) dielectrics may mitigate this problem. But the integration of these materials into integrated circuit fabrication is a complex task requiring material and new techniques. Moreover, it has also material limits due to chip area and minimal power requirements. New technology such as RF wireless interconnection using integrated antenna, transmitter and receiver is proposed for intra/interchip clock and data distribution [1, 2]. This future wireless interconnection essentially will form a local area network (LAN) as shown in Fig. 1 on a chip or among different chips. For high data transmission rate and multiple access capability of this wireless interconnection system, it requires wideband characteristics of each component [3]. A fully integrated time-hopped (TH) UWB transmitter and its pulse generation circuit for wireless interconnection in future ULSI is developed and presented in this paper.

2. TH-UWB transmitter

The circuit schematic of time-hopped UWB transmitter is shown in Fig. 2. TH-UWB transmitter first generates a typical time shifting or time hopped with pulse position modulation pulse and this pulse is then used to generate UWB signal. A typical UWB signal generated by the kth transmitter (i.e. kth user or kth chip) is given as [4]

\[ s(t) = \sum w_i(t - jT_i - \Delta f_{c_i}T_i - \Delta d_{c_i}) \]

Where, \( w_i(t) \) represents the transmitted Gaussian monocycle, \( T_i \) is the frame time, \( c_i \) is the hopping number, \( T_i \) is the chip rate, \( \Delta f \) is the modulation time and \( \Delta d \) is data (0 or 1). Here the time shifted pulse train is generated from the frame clock. The multiplexer selects the time shifted frame clock which is generated by the voltage controlled oscillator (VCO), divider and delay line, according to PN (pseudorandom) sequence with three hopping bits (i.e. hopping number \( c_i \) varies from 0 to 7). Here, eight channels are considered for initial investigation of the proposed system. Linear feedback shift register which consists of four clocked D-type Flip-Flop along with an exclusive-or logic as feedback is used to generate such PN sequence. The time shifting due to pulse position modulation (PPM) to encode data is done by the fine delay line which provides a delay of approximately the modulation time (0.05ns). Two to 1 multiplexer finally selects the time shifted pulse train due to PN sequence and PPM according to data symbol (“0” or “1”). The time shifted pulse train is then used to produce monocyte pulse with wide bandwidth by monocyte pulse (MCP) generator. It consists of RLC network with RC filter, pass gate and pulse generation circuit for generating the short rectangular pulse (SRP) and gate control pulse (GCP) [5].

3. Monocyte pulse measurement

The test chip of monocyte pulse (MCP) generator shown in Fig. 5 is designed and fabricated by using TSMC 0.18 µm CMOS mixed signal process. The die microphotograph of the circuit is shown in Fig. 3. The MCP generation circuit occupies an area of 0.19mm2. The fabricated chip is bonded on a test PCB as shown in Fig. 6.

The measurement system consists of Agilent 81134A pulse pattern generator, infiniium digital oscilloscope and dc power supply. The SRP of width 0.1ns and GCP of width 0.5ns as shown in Fig. 7 are applied to MCP generator by using pulse pattern generator. Both applied pulses has equal rise and fall time of 70ps with a repetition rate of 400 MHz. The monocyte pulse is measured by infiniium digital oscilloscope and is shown in Fig. 8. The fig. 8 shows that the measured monocyte pulse is not symmetric because of low amplitude of negative part which may be due to the effect of high distributed parasitic resistance. The simulation also confirms this effect as shown in Fig. 9 where the black curve is the simulated monocyte pulse for the same inputs and without considering the effect of output pad buffer. The measured monocyte pulse width (1.13ns) as shown in fig. 8 differs from the desired pulse width of 0.5ns. This is due to the effect of low frequency buffer of the TSMC output pad. To investigate this effect, the monocyte pulse generator along with low frequency output buffer instead of TSMC output pad buffer is simulated. The simulation result as shown in red curve of fig. 9 depicts the same effect as found in measurement. The absence of asymmetric in this case is due to not considering the output pad parasitic effect.

4. Conclusion

We developed and fabricated a single chip TH-UWB transmitter by using 0.18 µm CMOS technology and its performance is analyzed by simulation. UWB transmitter pulse generator circuit which generates monocyte pulse is tested and measurement result is presented. The measurement results show that the monocyte pulse can be generated from RLC network along with RC filter and pass gate from the time hopped signal.

References

Table I: Transmitter performance data

<table>
<thead>
<tr>
<th>UWB system</th>
<th>Time hopping Impulse</th>
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<tbody>
<tr>
<td>Carrier Frequency</td>
<td>No carrier</td>
</tr>
<tr>
<td>Transmitter Signal bandwidth</td>
<td>3.3 GHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>50 Mbps</td>
</tr>
<tr>
<td>Single Channel datarate</td>
<td>400 Mbps</td>
</tr>
<tr>
<td>Modulation</td>
<td>Pulse position modulation</td>
</tr>
<tr>
<td>Average power consumption</td>
<td>12.5 mW</td>
</tr>
<tr>
<td>Architecture</td>
<td>All digital except pulse generator</td>
</tr>
<tr>
<td>Technology</td>
<td>TSMC 1.8v, 0.18 µm CMOS mixed signal process</td>
</tr>
<tr>
<td>Implementation</td>
<td>Single chip</td>
</tr>
<tr>
<td>Circuit Size</td>
<td>0.729 mm² (excluding antenna)</td>
</tr>
<tr>
<td>Application</td>
<td>Short distance (on chip wireless interconnection for future ULSI)</td>
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</tbody>
</table>

Fig. 1 Wireless interconnect system for future ULSI (a) Intrachip and (b) Interchip.

Fig. 2 TH-UWB Transmitter Schematic.

Fig. 3 (a) Die Microphotograph; (b) TH-UWB transmitter layout.

Fig. 4 Simulation output: (a) Delayed frame; (b) Three hopping bits; (c) RZ data [1 1 0 0 0]; (d) Multiplexers output (e) Monocycle Pulse (MCP) train and (f) FFT of monocycle pulse.

Fig. 5 Monocycle pulse generator with bonded wire and output pad buffer.

Fig. 6 Test setup for monocycle pulse generator.

Fig. 7 Input pulses from pulse pattern generator to generate MCP.

Fig. 8 Measured Monocycle pulse.

Fig. 9 Simulated monocycle pulse (considering bonded wire and output pad buffer).
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MOTIVATION
Advanced wireless interconnect system could be a solution for interconnect delay problem due to parasitic Resistance, capacitance and inductance in future ULSI

Wireless Interconnection

Requirement
- High Data rate
- Multiple access

CHIP MICROPHOTOGRAPH AND LAYOUT

TH-UWB TRANSMITTER

TH-UWB TRANSMITTER CIRCUIT SCHEMATIC

TH-UWB TRANSMITTER CIRCUIT SCHEMATIC

MONOCYCLE PULSE GENERATOR

CHIP MICROPHOTOGRAPH AND LAYOUT

CHIP MICROPHOTOGRAPH AND LAYOUT

HSPICE SIMULATION

HSPICE SIMULATION

CHIP MICROPHOTOGRAPH AND LAYOUT

CHIP MICROPHOTOGRAPH AND LAYOUT

SRP AND GCP GENERATION CIRCUIT

SRP AND GCP GENERATION CIRCUIT

MCP FROM SIMULATION

MCP FROM SIMULATION

CONCLUSIONS
- TH-UWB transmitter is designed and fabricated. Time-hopped signal due to PN sequence and PPM is generated from time shifted frame. Time shifting is performed by delay circuit. This is only necessary to keep constant delay with any variation of Vdd and substrate voltage.
- Monocycle pulse can be generated from RLC network with RC filter and Peak gate. The circuit can be implemented using the current CMOS technology which can be used to implement the TH-UWB transmitter in a single chip.
- Pulse width of generated monocycle pulse data rate of UWB transmitter because data rate is inversely proportional to the monocycle pulse width. Data rate can be increased by generating shorter pulse by using lower value of inductance in RLC network of TH-UWB generator.

ACKNOWLEDGEMENT
This work is supported by the Ministry of Education, Culture, Sports, Science and Technology, Japan under the 21st Century COE program at Hiroshima University.