Preface

The 21st century COE program “Nanoelectronics for Terra-Bit Information Processing” aims at the fusion of silicon-based nanodevices, circuits and integrated circuit-architectures. Fusion of the basic research fields is considered necessary for another goal of the COE, namely the construction of integrated systems with high-level recognition and learning functionality. Bringing up independent researchers which are capable of advanced, visionary and well reflected research in a broad range of fields is regarded as very important to accomplish our goals.

Our main specific research tasks can be summarized as:
* Unification of silicon-based system, circuit, device-modeling and device fabrication research
* Solution of the persistent 3-dimensional-integration problems by a wireless integration methodology
* Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures

Within the scope of the COE program, we hold workshops in the framework of the COE program to demonstrate our progress, to interact with worldwide leading groups for exchanging information as well as to initiate possible collaboration. The first workshop was held on March 17th in 2003 and presented an overview of the research fields in the focus of the COE. Lectures by outstanding leaders over the world were also given for verifying our concepts and enabling future interactions.

The 2nd workshop is held at Hiroshima University, the Graduate School of Advanced Sciences of Matter, Lecture Hall 401N. It focuses on the modeling and simulation tasks of the COE, aiming at providing opportunity to get an overview of present activities undertaken in the world. Requirement for simulations is increasing due to the complexity of device characteristics approaching technological limitations. More efforts are also requested to realize accurate SoC simulations. At the workshop possibilities to realize tight collaborations among different fields to accelerate the achievements are also discussed.

We would like to welcome you to the 2nd Hiroshima International Workshop on Nanoelectronics for Terra-Bit Information Processing. All of the COE members hope that this workshop will provide an opportunity for further interactions and discussions with you.

Atsushi Iwata
Leader of the 21st Century COE program on Nanoelectronics for Tera-Bit Information Processing
Director of the Research Center for Nanodevices and Systems
Hiroshima University
1-3-1 Kagamiyama, Higashi-Hiroshima 739-8530, Japan
E-mail: iwa@dsl.hiroshima-u.ac.jp
PROGRAM

PLENARY SESSION  9:00 – 15:40
Lecture Hall 401N, the Graduate School of Advanced Sciences of Matter

9:00  Opening Address
Taizo Muta, President of Hiroshima University

9:05  Overview & Keynote Address
- Recent Progress of the COE -
Atsushi Iwata, Director of the COE, Hiroshima University

9:15  [Invited] Low Power SoC Technology Development at STARC
Koichiro Ishibashi, STARC

10:15 [Invited] Quantum Mechanical Carrier Transport and Nano-scale MOS Modeling
Zhiping Yu, Tsinghua University, China

11:15 Wireless Interconnection on Si LSI using Integrated Antenna
Takamaro Kikkawa, Hiroshima University

11:30 [Invited] Physics-Based Modeling of Electro-Magnetic Parasitic Effects in Interconnects
Prof. G. Wachutka, TU München, Germany

12:30 – 14:00  Lunch Break

14:00  [Invited] Modeling CMOS Non-Quasi-Static Effects in a Quasi-Static Simulation Engine
Musun Chan, Hong Kong University, China

15:00  MOSFET Modeling for RF-CMOS Design
Mitiko Miura-Mattausch

15:40 – 16:00  Coffee Break

POSTER SESSION  by COE members  16:00 – 18:00
The 4-th Floor Lounge, the Graduate School of Advanced Sciences of Matter

P-1  A Multi-chip Vision System with a PWM-based Line Parallel Interconnection
Seiji Kameda, Mamoru Sasaki and Atsushi Iwata

P-2  Human Face Detection and Recognition using Principle Component Analysis
H. Ando, N. Fuchigami, M. Sasaki and A. Iwata

P-3  Neural-Sensing LSI with Wireless Interface
Takeshi Yoshida, Takayuki Mashimo, Miho Akagi and Atsushi Iwata
P-4 CDMA Communication Chips for Highly Flexible Robot Brain
Mitsuru Shiozaki, Toru Mukai, Mamoru Sasaki and Atsushi Iwata

P-5 A Single Chip UWB Transmitter Based on 0.18-μm CMOS Technology for Wireless Interconnection
Pran Kanai Saha, N. Sasaki and T. Kikkawa

P-6 A Single Chip UWB Receiver based on 0.18-μm CMOS Technology for Wireless Interconnection
Nobuo Sasaki, Pran Kanai Saha, and Takamaro Kikkawa

P-7 A Wireless chip interconnect using resonant coupling between spiral inductors
Mamoru Sasaki, Daisuke Arizono and Atsushi Iwata

P-8 Low-Power Digital Image Segmentation of Real-Time VGA-Size Motion Pictures
Takashi Morimoto, Yohmei Harada, Osamu Kiriyama, Hidekazu Adachi, Tetsushi Koide, and Hans Jürgen Mattausch

P-9 A Strategy Learning Model for Robot Brain
Masahiro Ono, Mamoru Sasaki and Atsushi Iwata

P-10 Chip-Architecture for Automatic Learning Based on Associative Memory and Short/Long Term Storage Concept
Masahiro Mizokami, Yoshinori Shirakawa, Tetsushi Koide, and Hans Jürgen Mattausch

P-11 Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search with Large Reference Pattern Number
Yuji Yano, Tetsushi Koide, Hans Jürgen Mattausch

P-12 Improved Mixed Digital-Analog Nearest-Match Circuit for Fully-Parallel Associative Memories
Kaji Mujibur Rahman, Kazuhiro Kamimura, Tetsushi Koide, and Hans Jürgen Mattausch

P-13 Towards Current-Characteristic Simulation of p-i-n Photodiodes based on Spectral Method

P-14 1/f and Non-1/f Low Frequency Noise Measurements and their Modeling with HiSIM

P-15 Optical Properties of Ring Resonators on Si Chips
Yuichiro Tanushi, Masaru Wake, Keita Wakushima, and Shin Yokoyama
P-16 Study in Structure and Fabrication Process of 3-Dimensional CMOS Transisto
K. Okuyama, K. Kobayashi, S. Matsumura, and H. Sunami

P-17 Multiple-Step Electron Charging in Si Quantum-Dot Floating Gate nMOSFETs
Mitsuhisa Ikeda, Yusuke Shimizu, Taku Shibaguchi, Hideki Murakami and Seiichi Miyazaki

P-18 Characterization of Electronic Charged States of Single Si Quantum Dots with Ge Core Using AFM/Kelvin Probe Technique
Yudi Darma, Kohei Takeuchi and Seiichi Miyazaki

P-19 Local Characterization of Electronic Transport in Microcrystalline Germanium Thin Films by Atomic Force Microscopy Using a Conducting Probe
Katsunori Makihara, Yoshihiro Okamoto, Hiroshi Nakagawa, Mitsuhisa Ikeda, Hideki Murakami, Seiichiro Higashi and Seiichi Miyazaki

P-20 Atomic layer deposition of HFO_{2} for gate dielectrics
Yuichi Yokoyama, Hiroyuki Ishii and Anri Nakajima

P-21 Workfunction Tuning for Single-Metal Dual-Gate CMOS with Mo and NiSi Electrodes
K. Sano, M. Hino, and K. Shibahara

P-22 Etching Properties and Optical Emission Spectroscopy of NH_{3} Added C_{5}F_{8} Pulse-Modulated ICP Plasma
Masahiro Ooka and Shin Yokoyama

CLOSING REMARKS

18:00  Prof. Mitiko Miura-Mattausch