Perspective on Emerging Devices and their Impact on Scaling Technologies

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Abstract
We review and discuss the latest developments in FinFETs as an emerging device and its impact on scaling technologies.

Introduction
Transistor scaling has been the major driving force in the semiconductor industry for 40 years. The track has been one of many roadblocks and creative solutions. Most FinFET reports focus on devices; here we discuss technology opportunities and challenges.

The microelectronics industry is constantly seeking ways to scale transistor dimensions in order to allow for more transistors on a single chip, to scale down capacitance and to keep the drive current high while the voltage supply is scaled down to reduce power consumption. When scaling conventional planar devices below the 65nm node, short-channel effects (SCE) start to dominate over the device performance. Increased gate control is achieved by reducing the gate insulator thickness, by reducing the depth of S/D regions, and by increasing channel doping. All three strategies have major disadvantages: an increase gate leakage, an increase in the parasitic S/D resistance, a compromised carrier mobility and S/D leakage. Another approach to improve gate control over the channel is by using multiple gate devices [1,2]. It is projected that these 3-D device architectures may start to replace planar MOSFETs for specific applications in the 32nm node and beyond [3].

FinFET process
Because the 32nm node does not exist yet, FinFETs are built with existing higher node processes. In this work, we choose to start from a standard 130nm process with an extension towards a 45/32nm seized 6T-SRAM cell.

Fin patterning
A typical FinFET process flow is presented in Fig.1. Most of the work to date is based on SOI substrates [4,5], although bulk FinFETs [6,7] have been reported. An opportunity of SOI substrates is the ability to work with mesa-type active areas due to the insulating nature of the buried oxide (Box) [8]. The opportunity is that one avoids the need for an STI process and enjoys immunity to latch-up. Several challenges exist. A typical test structure for a FinFET is shown in Fig.2. The various fins are connected through the use of a S/D pad. Despite the fact that they are a convenient way of connecting the multiple fins, they require sub-resolution resist openings to be printed. The rounding of the resist opening increases the Wfin as Lfin reduces and can be mitigated by advanced illumination conditions and OPC (see Fig.3). It can be avoided by strapping the fins with a local interconnect Metal-0 (see Fig.4), at the expense of extra process complexity. From a lithography point of view, the problem of resist corner rounding is the shifted to a line shortening, which is believed to be much more manageable by OPC. A second, related issue is the use of advanced illumination conditions, like dipole [9], and their layout restrictions like forbidden pitches and uni-directionality.

As technologies scale sub-45nm, uni-directionality in layout style may be required to help maintaining the lithography process window. FinFETs provide a great opportunity because by nature they favor single direction, CD and pitch, and provide therefore a regular (like DRAM) style layout to make logic circuits. Fig.5 shows a typical 6T-SRAM active areas pattern with 150nm pitch with and w/o OPC correction [9, 10].

Gate patterning
The opportunities provided at the fin level create some challenges at the gate level, mainly due to the extra topography. A first challenge is that, depending on the fin height (Hfin), the process window for gate etch may shrink significantly. A typical non-optimized process yields poly residues from micro-marking (see Fig.6). One opportunity is the use of the ‘poly etch-back` process (see Fig.7) leading to a smoother poly-edge preventing any HM micro-masking and hence residues.

A second challenge is the CD uniformity as the gate runs over a fin. Fig.8 (top) shows two examples of logic gates indicating the loss of CD control over narrow fins (Wfin=35nm). The opportunity arises from BARC etch optimization combined with ‘topography-dependent OPC’ leading to a much improved process (Fig.8 bottom). A particular challenge is the simultaneous integration of logic and SRAM style circuits in sub-45nm nodes [9], particularly combined with spacer defined fin patterning.

Metal Gate and Vt tuning
A major challenge in the case of any narrow active area device, including multi-gate devices, it the difficulty to tune the threshold voltage by means of channel doping. Extremely high doping concentrations are needed for narrow-fin devices, exceeding 5e18cm^-2, to have any sizeable effect on V_T as shown on Fig.9. This raises concerns of V_T fluctuations due to random dopant distribution, significant mobility degradation and junction leakage. In addition, the V_T of highly doped fins is sensitive to variations in Wfin (Fig.10).

The opportunity lies in effectively making use of double gate effect to control short channel effects (SCE) combined with tune-able metal gates (MG). Undoped channels maximise mobility, sub-threshold slope and Vt control. Ideally one would use a single n-type (or p-type) metal that is selectively tune-able (implant of C, N, F,...) towards p-type (or n-type). Inserted midgap metals like TaN and TiN have been demonstrated on FinFETs [9,11,12,13] as shown in Fig.10. The use of fully silicided (FUSI) gates in FinFETs has been demonstrated [14] and provides MG action with low Vt’s by use of NiSi phase control [15,16] or alloying.

45/32nm circuit aspects
FinFETs have been integrated into various SRAM cell seize [17,18] down to 0.274um² [9] using optical litho (Fig.12). The cell concept has been shown to scale below 0.14um² [19].

For reasons of cell stability and speed, one needs to design proper beta ratios. Opportunities to modulate the beta ratio are choosing different L’s, selectively etching back the Hfin differently over nFET and pFET regions and selecting the right starting substrate surface and notch position.

Recently, the use of channel strain to boost drive currents in bulk and SOI technologies have been demonstrated [20,21]. Initial results on FinFETs have been reported [22], but more work is required to match current state-of-the-art CMOS.

Another opportunity, that requires more in depth study, is the potential to optimize the technology for A[um²] rather than the traditional A[um]. Very high current densities can be achieved by increasing the Hfin that may enable different architectures to be optimal (eg, BEOL loaded circuits).

References
[5] J.B. Doyle, Symp. VLSI Tech 2003, p.113
[18] T. Park, IEDM 2003, p.27
- Mesa-type fin patterning
- Surface repair + conditioning
- Gate deposition + patterning
  - 1.4nm HfO2
  - 5nm TiN
  - 100nm polysilicon
  - 193nm photo, gate etch
- Extension/HALO implant
- HDD Spacer
- deep S/D implant
- Spike anneal
- NiSi formation

Fig. 1 Simplified FinFET process flow

Fig. 2 SEM image of a mesa-type active area

Fig. 3 Wfin as function of Lfin

Fig. 4 Two different ways of connecting fins, (top) active areas (bottom) local interconnect M0.

Fig. 5 Fin CD for standard process (a) and OPC optimized process (b)

Fig. 6 FinFET after gate etch, (top) with non-optimised etch process, (bottom) with optimized process (etch back)

Fig. 7 Cartoon showing standard (top) and poly etch-back (bottom) process.

Fig. 8 Gate CD variation over fin topography, (top) examples of standard process in logic area, (bottom left and right) optimized process in logic and 0.3um2 SRAM cell

Fig. 9 2D Device simulation result indicating the sensitivity of Vt to channel doping for 3 different device architectures and work function.

Fig. 10 Measured nFET Vlin as function of Wfin for various channel doping levels.

Fig. 11 TEM showing Fin with inserted TiN / HfO2 gate capped with 100nm amorphous-Si.

Fig. 12 Tilted SEM of a 45nm node SRAM cell with FinFETs
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Outline

✓ Introduction
✓ Fin patterning, 6T-SRAM cell fabrication
✓ Gate patterning, MG and Vt tuning
✓ Conclusions

How it all got started...

1947
The Point contact transistor
Bell Labs

1958
The First IC
Texas Instruments

1961
The First Planar IC
Fairchild

A Few enabling R&D Breakthroughs

Scaling Trends

Power - Performance

Introduction of Channel Strain at 90nm and beyond allows to meet chip performance with less aggressive scale of Lg and Tox
After investigation:
- Performance ~ CV/I
- Power (Iddq) ~ Ioff*V

Traditionally:
High Idsat => Thin Tox

However,
Thin Tox limited by gate leakage

New paradigm (2003-beyond):
High Idsat => High mobility
=> Low Rd

Device Design Parameters
Opportunities:
1. Rd => Strain, USJ & silicide
2. µ => Strain, orientation, Ge
3. Tinv => Metal Gate, High-K
4. Lg => Architecture
5. Cpar => SOI, Tgate, Spacer

Any new CMOS family member is working on 1 or more of these.
Device Architecture

From Bulk to SOI to Multi-Gate

- Short channel effect
- Double gate effect
- Sub-threshold slope
- Stronger gate-channel coupling
- Mobility
- Lower channel doping

Device scaling

Bulk scaling
+ strain
- High doping levels

Device Architecture

FinFET (DG) fabrication

Ring Oscillators
Co-design of TCS

Improved loop: more internal feedback is needed at the various levels, with the adding of the DEVICES (wires and Xtors) at the tech. level

Feedback

Conventional scaling

Expectation:
- Substrate: Si, SOI, Ge, GaS, InP...
- Gate stack: SiO2, HK, poly, Metal Gate...
- Architecture: Bulk, PO-SOI, FO-SOI, InFET...

Models become more complex capturing the Physics, but remain abstract for designer

SPICE model

FinFET benefits

- Device
  - Scaling Lg (improved SCE immunity)
  - Higher drive
  - Maintain CV/I improvement 25% per node
- Circuit density
  - 1 direction
  - 1 fin & gate density
  - 1 W
  - No STI isolation issues (stack nFET/pFET closer)
- Architectural (high speed)
  - Opportunity to improve Vth bulk (Hfin can be increased)
  - What is the benefit in case BEOL RC does not scale?
- Process technology
  - Compatibility with std processing

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- Introduction
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Process sequence

Mesa-type fin patterning
Sidewall conditioning
Gate deposition + patterning
- 0.4nm chemox
- 1.4nm ALD-HfO2
- 5.0nm ALD TiN
- 100nm poly-Si
- 193nm photo gate etch + strip
- Extension/HALO
- H0D spacer
- Raised S/D epi
- Deep S/D + spike RTA
- NiSi
- CA/M1

FinFET follows conventional processing, can be done in any Si pilot line.

Process re-useability is higher than 70%.

New steps:
- HK / MG
- raised S/D epi
- (-spacer defined fin)

Fin patterning

2 approaches
- Resist-defined fin (conventional)
- Spacer-defined fin

Resist-defined

Spacer-defined

Hard Mask
- TEOS, SiN or SiON, APF (C-based)
- Used for CD trimming
- Issues:
  - Removal creates box recess
  - Too much trimming creates LER

Photo process
- 193nm, altPSM for optimum process control and resolution
- CD control

Etch process
- Modified gate etch process (Hfin=30-60nm)
  - X-talline Si instead of poly-Si
  - Stopping on thick BOX

Strip process

Fin conditioning
- 2nm oxidation
- H2 anneal @900C

Fin patterning

Resist-defined

CD 10-20nm
Corner rounding
H2 anneal @900C

Bulk CMOS gate etching know-how can be Re-used to etch fins
Fin patterning
Resist-defined

Fin width depends on Fin length

Need for advanced litho settings & OPC

Dry 193, conventional illumination, No OPC
Wet 193, Quasar illumination, OPC

Extract more data out of the image: LER
Spacer defined patterning looks promising in this phase of device development because:

1. Less LER expected
   - pattern defined by spacer not by resist

2. Fin density is doubled
   - relaxes requirements on lithography
   - or more I/dsat per unit area (V/I instead of C/V/I)

3. Less CD variation expected over the wafer
   - spacer material & deposition parameters can be easily optimized (no dopants in place yet)
   - allows to optimize for the fin etch and surface smoothness (no trimming needed)

Spacer-defined fins always come in closed loops.

2 approaches
- Resist defined
- Spacer defined

Circuit aspects (resist-based)
- Typical device test layout
- SRAM cell
- Logic library elements (NAND, ...)

Typical device test layout
- fins are connected by a fin pad
- 1 contact would be OK

Typical 6T-SRAM layout
- stand-alone fins
- each fin need a contact

- Fin width independent of fin length
- line end shortening (manageable?)
- 0 need for metal-0 to connect fins and maintain density (M1 routing)
Fin patterning
Resist-defined

0.186μm² cell
pitch = 124nm
ASML /1250i, NA=0.85
immersion

0.134μm² cell
pitch = 112nm
ASML /1400, NA=0.93

Fin process shows excellent scalability

SRAM patterning
Resist-defined

SRAM cell size roadmap

45nm SRAM
X=730nm
Y=430nm
0.314μm²

Cell cross-sections

Typical device test layout
- fins are connected by
  a fin pad
- 1 contact would be OK

Typical logic library element
- stand-alone fins
- each fin need a contact

Modified logic library element
- stand-alone fins
- Metal-0 local interconnect
- only 1 contact needed
Outline

- Introduction
- Fin patterning, 6T-SRAM cell fabrication
- Gate patterning, MG and Vt tuning
- Conclusions

Gate patterning

- High topography gate formation
  - Ex. Micro masking by HM

Gate patterning

- Etch-back approach
  - deposit 200nm poly
  - anisotropic etchback to 100nm
  - litho + gate etch
  - deposit 100nm poly
  - anisotropic
  - idem (same recipes)

Threshold Voltage control

- Various fin doping
  - N+ poly gate
- Target Vt range
- Undoped fin

Threshold Voltage control

- Various fin doping
  - N+ poly gate
- Target Vt range
- Undoped fin
- Need MG (midgap +/- 200mV ?)
Gate patterning

**Metal Gate**

- **Bulk FET**
- **MuGFET**
- **Poly-Si**
- **SiON**
- **Si-fin**

**Gate patterning**

- **Poly-Si**
- **TaN, TiN, W, Mo,...**
- **SiON, HfO2**
- **Si-fin**

**Mobility improvement**

10-15% improvement in drive current from implementation of CESL with strain

Implementation of SiGe S/D into MuGFET increases 25% PMOS performance (Rs reduction + compressive strain)

**Conformal junctions**

PLAD proved to form conformation junctions*

Transistors with PLAD junctions demonstrated

20nm reduction in Lmin in NMOS and PMOS devices with PLAD

* As data

For Narrow FIN (~20nm):
- Excellent PMOS demonstrated on (HfO2/TiN/poly)
- Ion uncertainty from k-line Wfin measurements evaluated to be ~ +/- 7%

For Narrow FIN (~20nm):
- NMOS is fairly weak, in regards to this gate stack
- More characterization on going to better quantify drive loss from such narrow FIN (Rext)

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Tensile vs. compressive mobility improvement

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<th>Mobility gain</th>
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20nm reduction in Lmin in NMOS and PMOS devices with PLAD
Outline

- Introduction
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Summary

- FinFETs can be made with conventional processing
- Show excellent scalability, devices & circuit density
- Remaining issues
  - Idsat improvement
  - Introduction of strain
  - Junction engineering w/o defects
Metal gate for 3D-SOI devices

Gate & Fin patterning

Metal gate for 3D-SOI devices

Observation: GIDL

HARMONY++, BS20

BS20
0.186um2 cell
PC pitch = 150nm
/1250i

Poly residue
Poly etch back for smooth topography

2D Simulation study (Lg=25nm)

SOI MuGFET Device Roadmap

Program Status

We have a established baseline process

We have demonstrated 45nm node devices

We have demonstrated 45nm node circuits (SRAM cell)
Program Status

We have established a baseline process
- Route available
- Draft Design Rule manual available
- V0.1 SPICE model available
We have demonstrated 45nm node devices
We have demonstrated 45nm node circuits (SRAM cell)

Program Status & Highlights

We have demonstrated 45nm node devices
- Contain all the gizmos: HK/MG/Strain/Conformal USJ/…
- pFET OK, nFET low on Idsat
We have demonstrated 45nm node circuits (SRAM cell)

Program Status & Highlights

Highlights: baseline process

Objective: open up the window for gate etch optimization

Before:
Now in POR: polySi etch back

Residue free etch back

Program Status & Highlights

BLUES (preliminary floor plan)

Program Status & Highlights

We have established baseline process
- Route available
- Draft Design Rule manual available
- V0.1 SPICE model available
We have demonstrated 45nm node devices
- with HK/MG/Strain/Conformal USJ/…
- pFET OK, nFET low on Idsat
Actions in place to get improved performance
We have demonstrated 45nm node circuits (SRAM cell)
Short term Plan (2H05)

- nFET Idsat improvements
  - Gate process
    - EOT scaling from 2.1nm towards 1.3nm ... 1.1nm ...
    - 0-notch gate TiN process
    - Vt tuning strategy (implant, anneal)
    - Other MG candidates (Mo-based, W-based, WSi...)
  - Junction process
    - Conformal junctions by Plasma Doping, density scaling
    - Laser anneal
    - Raised S/D by SEG
  - Mobility
    - High stress CESL
    - Different orientation substrates
  - Silicide
    - NiSi, PtSi, YbSi

Program Status & Highlights

- We have a established baseline process
  - Route available
  - Draft Design Rule manual available
  - V0.1 SPICE model available
- We have demonstrated 45nm node devices
  - with HK/MG/Strain/Conformal USJ...
  - pFET OK, nFET low on Idsat
  - Actions in place to get improved performance
- We have demonstrated 45nm node circuits (SRAM cell)
  - Demonstrated 0.274µm² cell with Tan/SiON
    - In progress 0.245µm² with TiN/HfO2 : 200mm
    - Plan for 0.180µm² in place (193i) : 300mm
  - Printed (optical) Active Area (AF,RX) consistent with 0.13µm²

SC45-SC32 Status

- 1Q04 2Q04 3Q04 4Q04 1Q05 2Q05 3Q05 4Q05

SC32-1100 (15/12/2004)

- X=720nm
- Y=340nm
- 0.245µm²

SC32-1400 (20/1/2005)

- Active area printed on /1400 (NA=0.93, 300mm)
- Active Pitch 112nm
- Cell pitch compatible with 0.134um² cell

SC45+MG (23/12/2004)

- X=720nm
- Y=380nm
- 0.274µm²

Purpose of this work is to prepare the 1250i work

Process can be extended to aggressive pitches on /1100 due to aggressive OPC
EMERALD process learning

Highlights: Baseline process

Objective: reduce SCE in MUGFET transistor

Results:
- Better S
- Reduced DIBL

FIN scaled down to 20nm without loss in FIN height

Surface smoothening (H2 anneal)

- 850°C 5 min
- 900°C 2 min
- 900°C 5 min (POR)
- 950°C 1 min

Surface smoothening

H2 anneal vs no H2 anneal

Ioff [A/µm]

Objective: find a crystal-orientation independent technique of corner rounding

POR: Corner rounding achieved by H2 anneal only

Radius 10nm for 2nm SSE

Highlights: Baseline process

Objective: Increase FIN density for higher current /area

Spacer defined FIN patterning: feasibility proven for FIN doubling

Small CD (14-17nm) CD variations
Gate & Fin patterning (193nm resist)

SSDM 2005

Gate & Fin patterning (193nm resist)

SSDM 2005

Metal gate for 3D-SOI devices

MuGFET with MG

SSDM 2005

Solution: Berkeley approach with Si SEG

Si SEG on S/D after parasitic spacer recess ($H_{\text{gate}} > H_{\text{fin}}$)

SSDM 2005

Source/Drain Resistance ... (contd.)

Measurements on fabricated devices are shown Narrow fin MuGFETs show high S/D resistance ($R_{\text{SD}}$)

SSDM 2005

T1.1: SEG for MuGFET — faceting

SEG on MuGFET (no poly present):
- 45 nm grown on 60 nm height fins
- Facets are orientation dependent due to the difference in growth rate
- Epi overgrowth

SSDM 2005
**Highlights: Conformal junctions**

- Study on compatibility of different conformal USJ formation techniques with MUGFET structure started (PLAD, VPD, Solid Source, Epi tip, Schottky barrier, etc.)

**Novel Architectures**

- Compatibility and suitability of alternative annealing techniques (Flash, Laser) initiated.

**Poly 170 pitch, 6% AttPSM /1100, 0.75NA dry, CD in resist@BF**

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**OPC**

- Gap=50nm

- Gap=80nm

**STI process with flat topography**
Contact after litho

Gate & Fin patterning

Residue? Left over poly?

Gate patterning

Fin height reduction in small lines